

Specman Elite

Testbench Automation

Specman Elite

- ✓ Captures executable specifications
- ✓ Constraint-driven generation
- ✓ Data and assertion checking
- ✓ Functional coverage analysis
- ✓ SystemC support
- ✓ HW/SW co-verification support
- ✓ Support all major simulators

Functional verification is the bottleneck in delivering today's highly integrated electronic systems and chips. Verisity's Specman Elite® testbench automation solution gives you the industry's most powerful capability for automating the process of verification.

Specman Elite is a key component of Verisity's Verification Process Automation (VPA) solutions and blends third-generation process automation technology with world-class methodology to simplify verification. Specman Elite automates the entire verification process from the verification of individual blocks, to the full chip all the way to the project level, promoting productivity, quality and predictability.

Specman Elite

Verisity's Specman Elite is a comprehensive environment for all aspects of verification: automatic generation of functional tests, data and assertion checking, and functional coverage analysis.

But We Already Do That in 'C', VHDL, Verilog...

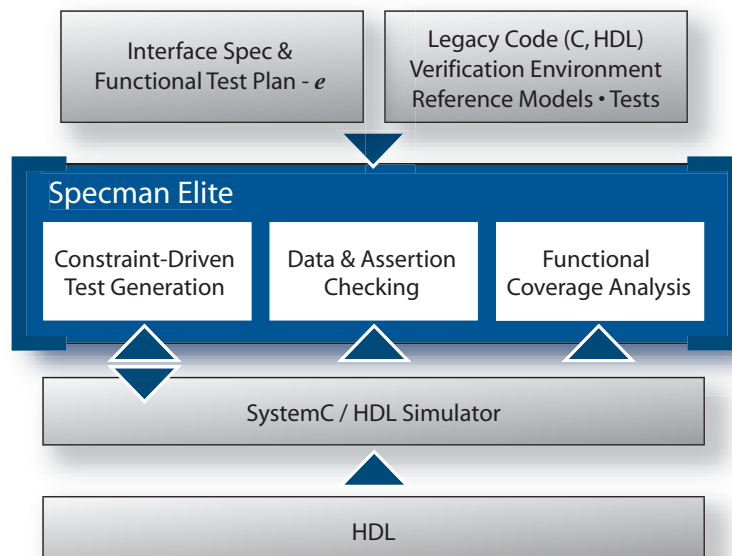
You may already have invested time and effort on internal solutions, but realistically these "tools" are rewritten project to project without allowing for significant reuse. They also don't contain the engines already built into Specman Elite, such as Verisity's patented Constraint Solver, which allows fast and easy test generation — built in!

The Verisity Solution

With Verisity's Specman Elite, you capture the rules from the specifications and use this info to automate the functional verification process. Specman Elite's methodology finds the "bugs you haven't thought of" in your design — caused primarily by ambiguities in the spec or unanticipated usage by the target system. The result? Faster verification and higher quality products.

Captures Executable Specifications

Our powerful *e* verification language allows you to capture the rules from specifications as well as generate tests automatically. Specman Elite eliminates misinterpretation of specifications.



Specman Elite helps drive the entire process of verification, from block, chip and system level, and project levels.

Specman Elite

Verity — Meet your SpeX

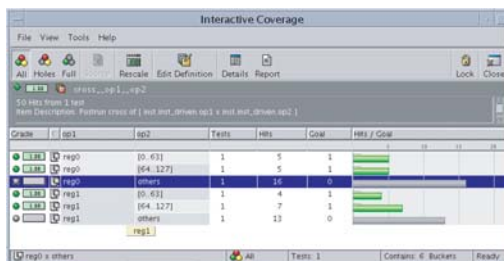
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For More Information

Please see us on the web at www.verity.com or contact your local sales representative for more information on SpeXsim and the complete SpeX Family of Verification solutions from Verity.



Functional coverage analysis allows you to identify holes and direct the entire process.

Constraint-Driven Test Generation

With Specman Elite's constraint-driven test generation, you can now automatically generate tests for functional verification. By specifying constraints, you can quickly and easily target the generator to create any test in your functional test plan. These tests can even be generated on-the-fly based on the current design state, making it possible to generate even hard-to-reach corner cases.

Data and Assertion Checking

Powerful temporal constructs enable you to capture complex protocols for assertion checking. On-the-fly data checking and generation allows context-specific expected values. You can use any combination of gray/black/white box checking to speed debugging.

Functional Coverage Analysis

An executable functional test plan measures the progress of verification. Functional analysis automatically identifies holes in the test coverage. Verification schedules become more predictable because functional coverage is a meaningful and direct measure of the completeness of your verification.

HDL Simulator Interfaces

All leading HDL simulators are integrated with Verity's Specman Elite. Internal signals of the device under test can be sampled and driven. 100 percent controllability and observability of otherwise inaccessible internal signals allows all engines of Specman Elite full access to signal values during the simulation.

SystemC Support

Specman Elite provides interface mechanisms to SystemC to allow driving and monitoring of Transaction Level Models (TLM) as well as signal level models. Established verification methodologies associated with Specman Elite may now be applied to the verification of SystemC architectural models using TLM, reference models including mixed SystemC and RTL environments, and co-verify SystemC models used for software development. Specman Elite provides interface adaptors for SystemC simulators including OSCI, Cadence NC-SystemC and CoWare ConvergenSC. With Specman Elite you create a single verification environment that can be used first to verify your SystemC model, and then re-used throughout the entire down-stream flow from RTL simulation to acceleration and emulation.

HW/SW Co-Verification Support

All leading HW/SW co-verification tools are supported. For example Verity's XoC™ and Mentor Graphics' Seamless™ co-verification environment are deeply integrated to enable functional testing of both hardware and software. Early integration and debugging of hardware/ software systems will eliminate errors and shorten time-to-market for the combined system.

