

SpeXtreme™

VPA for High-Performance Chip and System-Level Verification

SpeXtreme Benefits

- ✓ Dramatic increase in performance for chip and system verification
- ✓ Incremental and predictable flow to performance
- ✓ Reuse single verification environment from block to system and from simulation to emulation
- ✓ Accelerate best verification practices: Scalable Coverage Driven Verification, eRM, sVM
- ✓ Smooth transition to emulation

Functional verification is the number one bottleneck in delivering today's highly integrated electronic systems and chips. To address this challenge, Verisity offers solutions that combine automation with world-class technologies and methodologies to offer the most advanced, and unique, verification solutions. Called Verification Process Automation (VPA), these solutions solve the largest development bottleneck risk for customers.

Verisity's VPA solutions automate the complete process, from the block, to the chip and system levels, all the way to the project level where all verification activities are managed from the specification to closure. These solutions make up the SpeX Family of verification systems, which combines Verisity's VPA with complementary, world-class scalable infrastructure technologies.

SpeXtreme is a part of the SpeX Family of VPA solutions and provides high-performance verification for chips and systems. It integrates Verisity's SpeXsim™ with Xtreme®-II and RCC Compiler which combines direct RCC compilation, verification process automation, native compiled code mixed-language simulation and event-based acceleration and emulation.

Verification Process Automation (VPA) Systems	
vManager	PROJECT LEVEL Process and Verification Closure Management
SpeXtreme	HIGH PERFORMANCE CHIP AND SYSTEM LEVEL Acceleration and System-level Emulation
SpeXsim	BLOCK AND CHIP LEVEL Multi-level, Reusable VPA with Simulation

SpeXtreme is the highest performance verification system for chip and system-level verification.

SpeXtreme

Verisity's SpeXtreme is the most advanced verification solution for chip and system-level verification. It's easy to use, offers performance improvements of 20-100x by accelerating both the design and verification environment and provides a smooth transition to Mhz system-level emulation.

SpeXtreme's e RCC Compiler performs the direct compila-

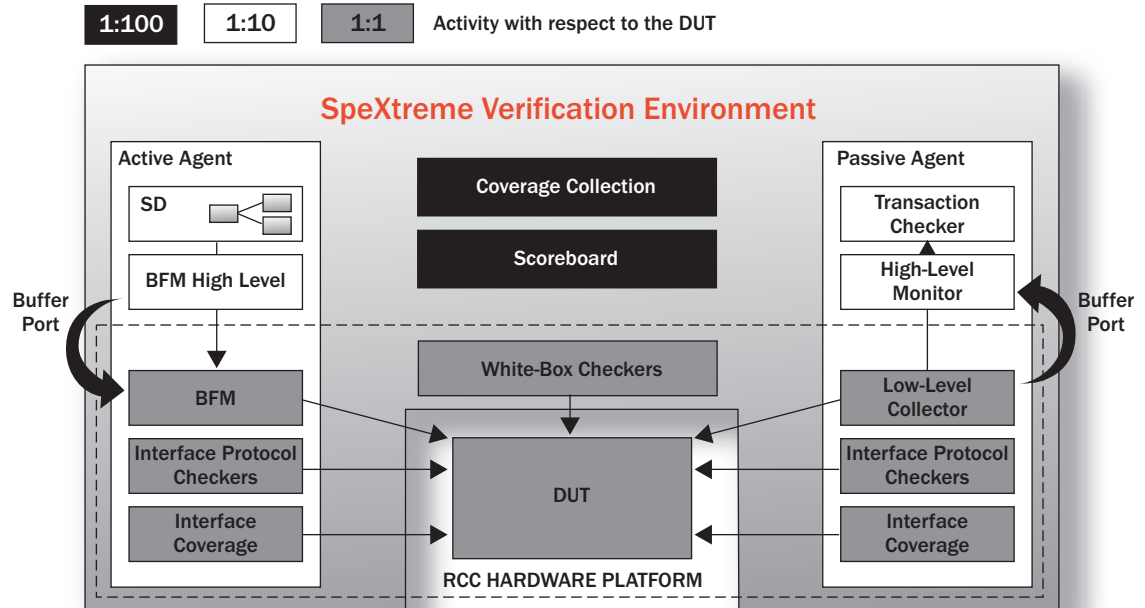
tion of e testbenches for acceleration onto the e behavioral processors of the Xtreme-II acceleration and emulation solution. High-performance execution is done through a direct kernel integration of Verisity's SpeXsim and Xtreme-II.

The combination of these world-class technologies brings users a more streamlined, integrated solution for chip and system-level verification.

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High Performance

SpeXtreme enables performance improvements of 20-100x by accelerating parts of the verification environment and by performing decoupled communication at the sequence level between SpeXsim and Xtreme-II. SpeXtreme also provides a smooth transition path to Mhz system-level emulation.

Reusable, Consistent Environments

With SpeXtreme, customers develop a single representation of their design that can be seamlessly used in simulation, acceleration and emulation. Similarly, customers develop a single verification environment, which they reuse throughout their verification process, not only moving up from block to chip and system

level, but also moving through the various technologies employed across the life of a project, from HDL simulation to acceleration to emulation.

Testbench Integration

SpeXtreme offers an incremental flow to performance. To get the best performance, customers can identify the parts of the verification environment which impact performance the most and compile them onto Verisity's behavioral processor technology. This technology enables high-level mapping of abstract testbench constructs into the Xtreme II hardware engine.

Coverage and Assertion Acceleration

SpeXtreme accelerates functional coverage and assertions directly onto the hardware box,

including assertions written in the emerging IEEE P1647 verification language standard based on *e*, and assertions imported from O-In Design Automation. In addition, Verisity plans to support the evolving design and assertion subsets of SystemVerilog and PSL.

Best Practices

SpeXtreme enables engineers to follow verification best practices and use Verisity's *e* Reuse Methodology (*eRM*™) and System Verification Methodology (*sVM*™) guidelines. Through *sVM*, SpeXtreme offers automated support for specifying and generating system-level scenarios and utilizes specialized algorithms to ensure scalability of capacity, performance and time-to-verification closure.