



## VPA for Block and Chip-level Verification

### SpeXsim Benefits

- ✓ Specman Elite methodology with integrated simulator
- ✓ Lowers simulation costs for Specman Elite users by approximately 50%!
- ✓ Open standard, multi-language support: Verilog, VHDL, e, SystemC
- ✓ Automates block and chip-level verification processes
- ✓ Seamless migration to event-based acceleration and emulation

Functional verification is the number one bottleneck in delivering today's highly integrated electronic systems and chips. To address this challenge, Verisity offers solutions that combine automation with world-class technologies and methodologies to offer the most advanced, and unique, verification solutions. Called Verification Process Automation (VPA), these solutions solve the largest development bottleneck risk for customers.

Verisity's VPA solutions automate the complete process, from the block, to the chip and system levels, all the way to the project level where all verification activities are managed from the specification to closure. These solutions make up the SpeX Family of verification systems, which combines Verisity's VPA with complementary, world-class scalable infrastructure technologies.

The first integrated product in the SpeX Family is SpeXsim™ which combines the testbench automation capabilities and proven processes of Specman Elite® with the third-generation simulation technology of Xsim® to provide a streamlined, integrated verification system for block and unit-level verification.

Verification Process Automation (VPA) Systems	
<b>vManager</b>	<b>PROJECT LEVEL</b> Process and Verification Closure Management
<b>SpeXtreme</b>	<b>HIGH PERFORMANCE CHIP AND SYSTEM LEVEL</b> Acceleration and System-level Emulation
<b>SpeXsim</b>	<b>BLOCK AND CHIP LEVEL</b> Multi-level, Reusable VPA with Simulation

SpeXsim is the most advanced verification solution for block and chip-level verification.

### SpeXsim

Verisity's SpeXsim is the most advanced verification solution for block and chip-level verification, combining testbench automation and native compiled code mixed-language simulation into one tightly integrated package. SpeXsim also supports packaging options that include Verisity's SureCov™ code coverage, as well as leading debug solutions such as Novas.

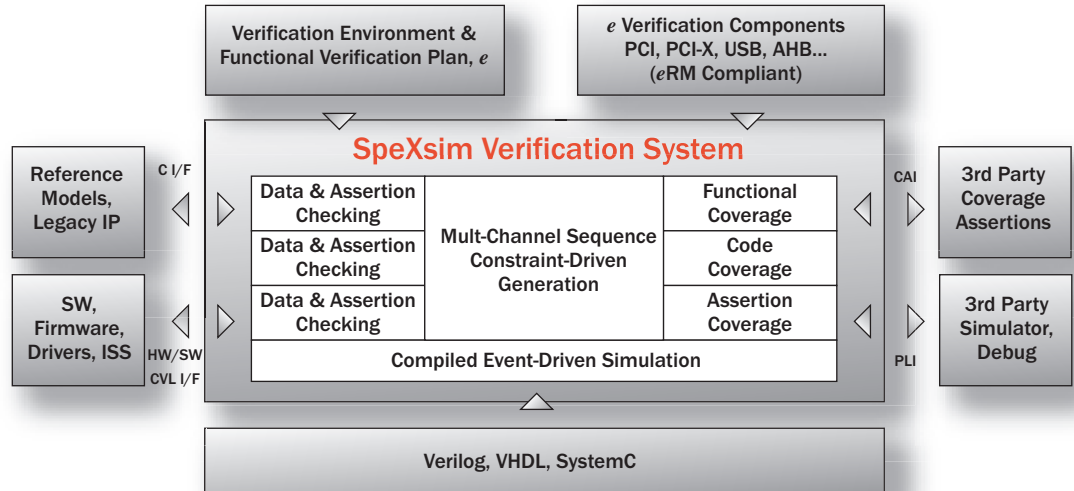
SpeXsim is a comprehensive environment for testbench automation, including automatic generation of functional tests, data and assertion checking, functional coverage analysis and HDL simulation control. SpeXsim supports the highest performance event-based simulation of standard HDLs, and seamlessly migrates the design from the workstation to high-speed hardware engines for acceleration, emulation

## Contact Information

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## The “Verification Backbone”



*SpeXsim is a complete verification system that drives you from specification to verification closure.*

and HW/SW coverification. The combination of these two world-class tools brings users a more streamlined, integrated solution for block and unit-level verification.

### Direct Kernel Integration

The direct kernel integration of Specman Elite and Xsim offers high performance, out-of-the box interoperability and ease of installation. In addition, SpeXsim is the only verification solution today that provides true scalability for system-level verification with the ability to run on the Xtreme® acceleration/emulation platform. This seamless integration provides the most flexible and accessible verification system, increasing your

verification productivity and confidence in your designs.

### Mixed-Language Support

SpeXsim simultaneously supports every current and proposed IEEE design automation standard, including VHDL, Verilog, SystemC and the emerging IEEE P1647 verification language based on *e*. Verisity also plans to support the evolving design and assertion subsets of SystemVerilog PSL, and O-In tools.

### Functional Coverage Analysis

SpeXsim’s executable functional test plan measures the progress of verification. Functional coverage analysis automatically identifies holes

in the test coverage. Verification schedules become predictable because functional coverage is a meaningful and direct measure of the completeness of your verification.

### Event-Driven Simulation

SpeXsim’s third generation, event-driven simulation engine delivers scalability and performance via a direct kernel interface to the embedded Specman Elite generation and coverage engines. And with built-in compatibility support for leading simulators, migrating your verification environment to SpeXsim can be accomplished with the setting of a switch.