

PCI Express *e*VC

Automated, Coverage-Driven Verification IP

PCI Express *e*VC

- ✓ Fully implements PCI-SIG compliance checklist
- ✓ Supports PIPE interface
- ✓ Supports power management (L and D states)
- ✓ Formats TLPs for request and completion transactions
- ✓ Implements credit based flow control
- ✓ Transaction ordering model and receiver buffer flow control
- ✓ Supports traffic class mapping over virtual channels
- ✓ Implements Data Link control and management state machine
- ✓ Generation and verification of TLP sequence number and LCRC
- ✓ Configurable TLP storage for Data link layer retry
- ✓ DCRC generation and verification of DLLP
- ✓ Implements acknowledgement and replay timeout mechanism
- ✓ Data scrambling, encoding and framing
- ✓ Supports multiple lanes (x1, x2, x4, x8, x16, x32)
- ✓ Clock compensation



e Verification Component Overview (*e*VC)

e Verification Components are reusable, configurable, pre-verified, plug-and-play verification environments. They offer the easiest to use, most complete module, chip and system level verification solution available. *e*VCs integrate automatic stimulus generation, assertion checking, and functional coverage analysis all within in a single, extensible component. *e*VCs drastically reduce the time needed to compose a verification environment.

The philosophy underlying *e*VCs differs significantly from alternative products. Rather than use thousands of directed tests, the *e*VC employs automatic generation and a coverage driven methodology. Using automated scenario generation the *e*VC can typically achieve 90%+ coverage of the protocol. With the addition of a few tests the remaining corner cases are then exercised. This approach uncovers more bugs faster and frees engineering time to focus on testing the DUT's proprietary functionality.

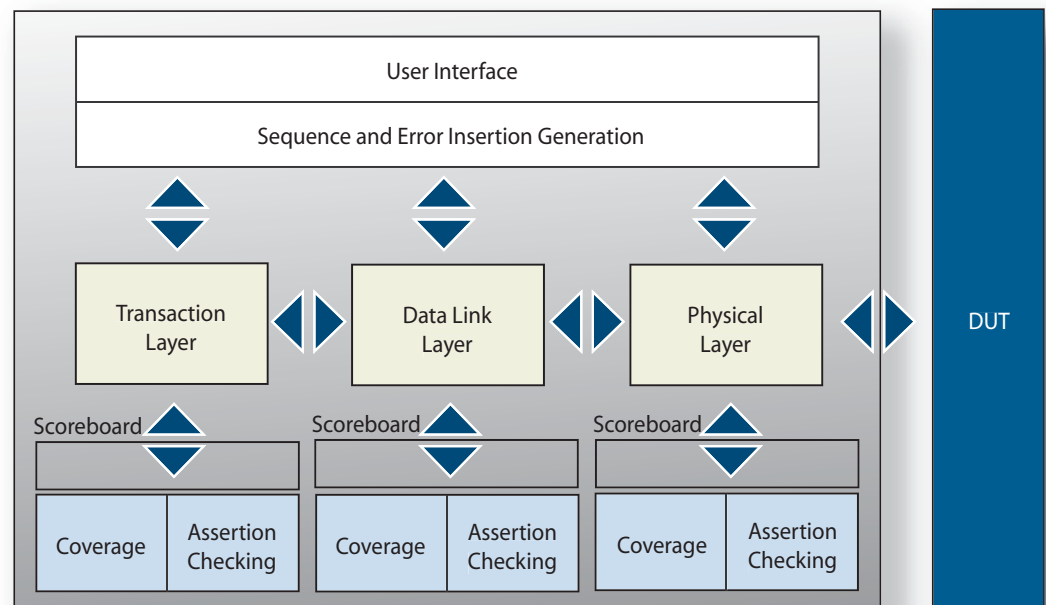
Quality and Productivity Gains

With *e*VCs verification environments are created in days instead of weeks or months. You can begin writing tests much earlier and achieve a much higher quality product. Furthermore, *e* Verification Components can be reused without expending any extra effort. This enables you to retain your investment when moving from module to system level verification as well as when verifying derivative products.

PCI Express *e*VC Overview

The PCI Express *e*VC is the only automated, coverage driven verification IP available. It comes from Verisity, the leading experts on functional verification. Verisity's PCI Express *e*VC verifies all three PCI Express protocol layers as well as any PCI Express end point or root complex.

Unlike HDL and C based BFM solutions, the PCI Express *e*VC encapsulates Verisity's Coverage Driven Verification methodology (CDV). The *e*VC includes a powerful automatic random sequence generator that automatically creates 90%+ of PCI



Block Diagram of the PCI Express *e* Verification Component.

PCI Express *e*VC

Verity – Meet your SpeX

Contact Information

Verity Design, Inc.
331 East Evelyn Avenue
Mountain View, CA 94041
PH: (650) 934-6800
FX: (650) 934-6801

www.verity.com



For More Information

To find out more about the PCI Express *e*VC contact your Verity account manager or distributor.

Express transactions and responses. The *e*VC's built-in functional coverage model and PCI-SIG compliance coverage suite provides clear reporting of what has and has not been covered. This frees engineers to focus on verifying coverage holes and the DUT's proprietary functionality, integration issues, corner cases and error scenarios.

Highly Configurable Verification Environment

The *e*VC can be used for functional verification of PCI Express devices such as end points and root complexes. Generation of every transaction type for all three PCI Express layers is fully supported. The *e*VC can also be configured to selectively enable or disable each layer, each functional block, as well as the functional coverage and checking mechanisms.

Major *e*VC Attributes:

- *e*RM, sVM, and VPA compliant
- Automated stimulus generation
- Supports Coverage Driven Verification (CDV)
- Includes PCI-SIG compliance coverage suite
- Validated against Intel's cBFM golden model

Deliverables

- Fully verified PCI Express *e*VC code written in the *e* language
- Documentation, including a user guide and release notes
- Standalone introductory demonstrations
- Sample, extensible tests covering basic functionality
- PCI-SIG compliance coverage suite

PCI Express *e*VC Functional Description

Sequence Generator	Provides constraint driven generation and synchronization of complex multi-transaction scenarios using eRM's sequence feature. Also includes interesting predefined scenarios that can be easily configured to your environment's specific requirements.
Transaction Layer Module	Supervises and controls the Transaction Layer.
Data Link Layer Module	Generates and manages DLL packets to ensure reliable packet delivery across the PCI Express data link layer.
Physical Layer Module	Generates symbols, scrambles data and maintains the Link Training and Status State Machine (LTSSM).
Functional Coverage Module	Provides highly configurable predefined functional coverage models enabling you to effectively analyze and report verification progress as well as the DUT's compliance level to the PCI-SIG compliance checklist
PCI-SIG Compliance Coverage Suite	The PCI-SIG Compliance Coverage Suite monitors packet traffic, device state and protocol activity and notifies you when violations occur. Unlike alternative solutions, it also enables you to determine exactly which PCI-SIG checklist items you have and have not covered in your simulations.
Scoreboard Module	TL, DLL and PHY layer scoreboard hooks enable the implementation of end-to-end and link-to-link scoreboards. In addition, performance and utilization analysis can be performed easily using the data provided by these scoreboard hooks.

