

PCI *e*VC

Automated, Coverage-Driven Verification IP

PCI *e*VC

- ✓ Supports PCI Bus Specification Revision 2.3
- ✓ Fully supports PCI compliance checklist provided by the PCI Special Interest Group
- ✓ Functions as one or more of:
 - Agent acting as target only
 - Agent acting as target and master
 - Arbiter
- ✓ Generates all types of PCI transactions (master) and responses (target)
- ✓ Supports memory modeling of all agent memory spaces (configuration/IO/Memory)
- ✓ Provides error injection with a wide variety of error types
- ✓ Supports 32-bit and 64-bit transactions
- ✓ Supports Message Signaled Interrupt (MSI) handling option
- ✓ Procedural interface (API methods) that allows a more directed scheme of transaction sending, specifically of configuration transactions
- ✓ Built-in bus traffic monitors
- ✓ Built-in coverage analysis for transfer types
- ✓ Scoreboard checking of input/output
- ✓ HDL independent

e Verification Component Overview (*e*VC)

e Verification Components are reusable, configurable, pre-verified, plug-and-play verification environments. They offer the easiest to use, most complete module, chip and system level verification solution available. *e*VCs integrate automatic stimulus generation, assertion checking, and functional coverage analysis all within a single, extensible component. *e*VCs drastically reduce the time needed to compose a verification environment.

The philosophy underlying *e*VCs differs significantly from alternative products. Rather than use thousands of directed tests, the *e*VC employs automatic generation and a coverage driven methodology. Using automated scenario generation the *e*VC can typically achieve 90-95%+ coverage of the protocol. With the addition of a few tests the remaining corner cases are then exercised. This approach uncovers more bugs faster and frees engineering time to focus on testing the Device Under Test (DUT) proprietary functionality.

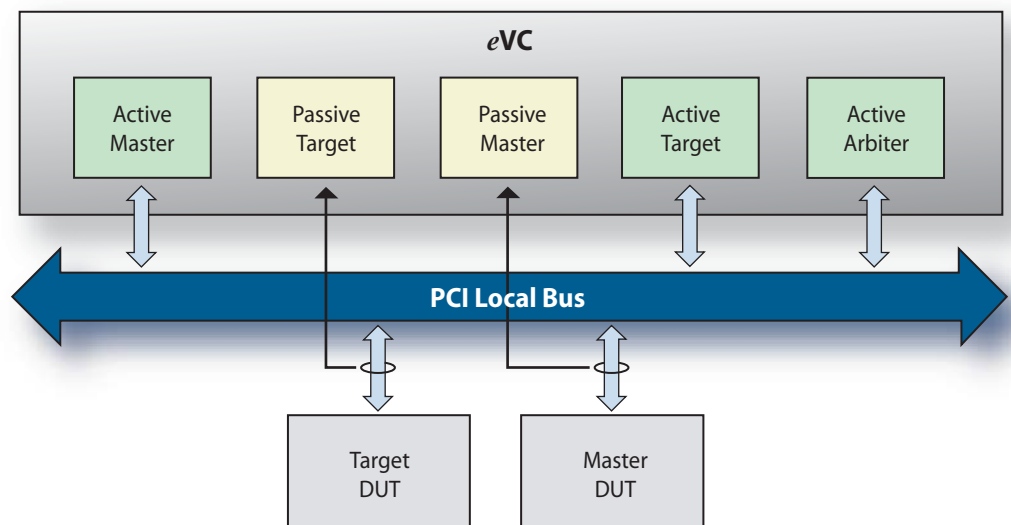
Quality and Productivity Gains

With *e*VCs verification environments are created in days instead of weeks or months. You can begin running tests much earlier and achieve a much higher quality product. Furthermore, *e* Verification Components can be reused without expending any extra effort. This enables you to retain your investment when moving from module to system level verification as well as when verifying derivative products.

PCI *e*VC Overview

The PCI *e*VC is an automated, coverage driven verification IP for PCI-based devices. It comes from Verisity, the leading experts on functional verification. Verisity's PCI *e*VC can be used to verify all PCI devices-master, target, arbiter and PCI-based systems.

Unlike HDL and C based BFM solutions, the PCI Express *e*VC encapsulates Verisity's Coverage Driven Verification methodology (CDV). The *e*VC includes a powerful automatic random sequence generator that automatically creates 90%+ of PCI transactions and responses.



Sample Configuration of the PCI *e*VC for a PCI sub-system verification.

Verity – Meet your SpeX

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For More Information

To find out more about the PCI eVC contact your Verity account manager or see us on the web at www.verity.com.

The eVC's built-in functional coverage model provides clear reporting of what has and has not been covered. This frees engineers to focus on verifying coverage holes and the DUT's proprietary functionality, integration issues, corner cases and error scenarios.

Highly Configurable Verification Environment

The eVC can be used for functional verification of PCI devices both at the module level, and system level. The eVC can be configured to instantiate any number of active masters or targets, as well as an arbiter. In addition, the eVC monitors any RTL agent for protocol correctness and coverage reporting. The eVC can also be configured to selectively enable or disable each functional block, as well as the functional coverage and checking mechanisms.

Major eVC Attributes:

- eRM, sVM, and VPA compliant
- Automated stimulus generation
- Supports Coverage-Driven Verification (CDV)

Deliverables

- Fully verified PCI eVC code written in the e language
- Full Documentation
- Standalone introductory demonstration
- Sample configuration and test case examples for master, target, arbiter and system designs

PCI eVC Functional Description

Active Master Agents	Active eVC masters request access to the bus, and then generate constrained-random transactions on the PCI bus. The eVC masters can generate every possible kind of legal transactions as well as a variety of erroneous ones (error injection).
Active Target Agents	Active target agents respond to transactions from masters by generating constrained-random responses. The eVC targets support configuration transactions and memory and IO address ranges. The eVC can generate every possible kind of legal responses as well as a variety of erroneous ones.
Passive Master and Target Agents	Passive eVC agents monitor the activity of DUT agents - masters and targets. Passive agents check that DUT agents adhere to the PCI protocol rules, and collect coverage on their activity.
Active and Passive Arbiter	The eVC can either instantiate an active arbiter or a passive one to monitor a DUT arbiter. The eVC active arbiter supports various arbitration schemes.
Functional Coverage Model	The eVC provides a functional coverage model based on the PCI bus traffic. Filling these coverage goals ensure that every possible traffic scenario on the bus was exercised for each DUT agent. The coverage model can be easily extended to monitor the actual functionality of the device, beyond the PCI interface.