



Verification Component Overview (eVC)

e Verification Components are reusable, configurable, and plug-and-play into verification environments. They model popular protocols, interfaces, processors, and embody the full Specman Elite® methodology. eVCs yield the fastest and most complete verification approach for each target protocol by delivering directed-random generation of transactions, full assertion checking, and functional coverage analysis of interesting transactions, scenarios, and events. In addition, since eVCs are plug-and-play components, you can intermix all eVCs that comply with the e Reuse Methodology (eRM) within your verification environment. eRM is a complete reuse methodology that codifies the best practices for eVC development.

e Verification Components provide numerous advantages including a major increase in productivity and higher quality products. With eVCs, verification environments are created in days instead of weeks or months. You can begin writing tests much earlier and complete verification faster.

e Verification Component reusability provides yet another major productivity advantage. For example, after performing module-level testing, the same eVC can then be used for top-level verification, enabling you to retain your training investment from project to project.

SATA eVC Overview

The eVC by IntelliProp is configurable, easy to install, and reusable. It meets current SATA-I and SATA-II specifications.

Verification Environment

For system level verification, the SATA eVC will test features of the phy, link, transport, and application layers. It can send ATA commands (to support existing host drivers), and is capable of testing the FIS Frames.

Deliverables

- Verified eVC code
- Documentation – user guide/release notes
- Test suite

Contact

For more information or to purchase please contact IntelliProp in the following manner:

Email: amits@intelliprop.com

Address:

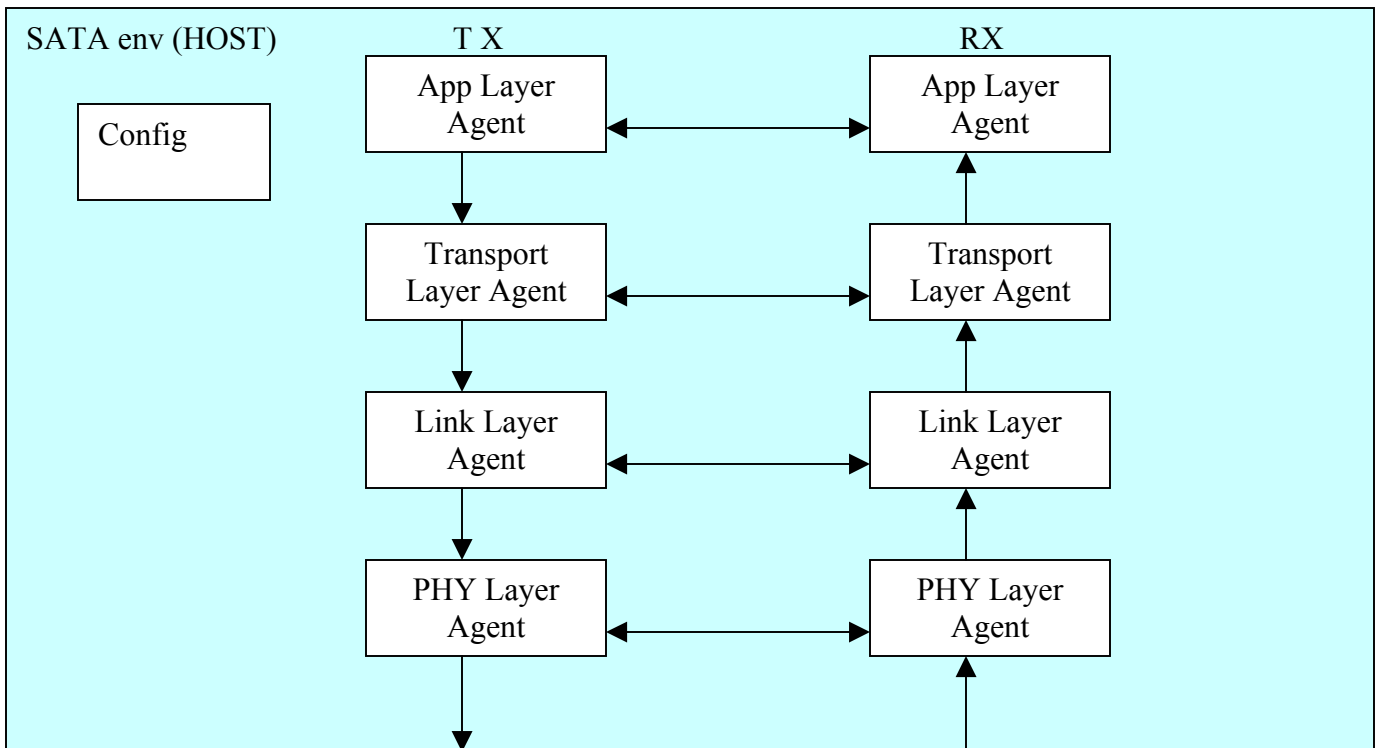
IntelliProp Inc.

4202 Fern Ave

Broomfield CO 80020

Functional Description

Component	Description
PHY Layer Agent	The PHY layer sequence sets up the connections and checks for timing when connecting to the DUT PHY and SERDES. This agent also includes Bus Functional Model to drive the HDL interface signals.
LINK Layer Agent	The LINK layer sequence transmits and receives frames after adding SOF, EOF and CRC to the FIS received from the TRANSPORT layer.
TRANSPORT Layer Agent	The TRANSPORT layer sequence constructs frame information structures (FIS) for transmission.
APPLICATION Layer Agent	The APPLICATION layer sequence for the HOST is the host bus adapter to support legacy parallel ATA commands. This agent also includes Shadow register unit that shadows contents of the device registers.



Features:

- Programmable as SATA Host model
- Programmable as SATA Device model
- Host model can perform legacy ATA command sequences
- Thorough checking of SATA-I and SATA-II features (selectable).
- Supports and checks for proper timing and misalignment errors in PHY.
- Supports primitive sequence generation and transmission at all layers.
- Configurable pattern generation for random, directed or erroneous patterns
- Configurable setup for scoreboard integration.
- Checkers will verify protocol timing checks and functional accuracy at each layer.
- Supports layered transmitter and receiver states
- Includes encoder/decoder, scrambler, and CRC checking.
- Built with eRM guidelines (scalable to test multi-port SATA hosts)
- Includes protocol coverage to show what protocol test have been produced

SATA eVC Architecture (Figure Above):

The figure shows the architecture of the SATA eVC configured as a SATA Host. A similar configuration is possible for the Device.

The connections to/from DUT are done via a bus functional model in the PHY layer TX agent that drives the HDL signals. There is an optional HDL interface at the link layer that can be used if the DUT has a link layer interface. Each agent in the TX side has sequence, sequence driver and a monitor (for coverage and protocol checks). Each agent in the RX side consists of a monitor that collects coverage and performs protocol checks. The lowest layer monitors on the TX and RX side listen to the traffic on the HDL interface to collect the transmitted or received information. The higher layer monitors derive the information from lower layer monitors. The RX monitors also communicate with the respective peer agent on the TX side if the sequence being sent has to respond to the information received on the RX side.

