



HDH 5000

RapidIO - e VERIFICATION COMPONENT (eVC)

HDH 5000 DATASHEET – NOVEMBER 2004 - PRELIMINARY VERSION 1.0

Overview

The process of developing appropriate verification environment for today's system-on-chip (SoC) designs becomes really hard, due to the fact that they include number of different protocols, peripherals, interfaces and processors. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, the reusability in verification has a very significant role. In order to increase verification productivity, huge verification environments are assembled from a number of verification components. Each of the verification components is designed for a specific protocol or architecture and is configured by the environment to produce desired behavior.

eVCs are e-Language Verification Components used for verification environments based on Verisity's Specman-Elite tool. They are reusable, configurable, easy to use and integrate into a verification environment. Their development is based one Reuse Methodology (eRM) defined by Verisity.

The RapidIO Interconnect Architecture, designed to be compatible with the most popular integrated communications processors, host processors, and networking digital signal processors, is a high-performance, packet-switched, interconnect technology. It addresses the high-performance embedded industry's need for reliability, increased bandwidth, and faster bus speeds in an intra-system interconnect. The RapidIO interconnect allows chip-to-chip and board-to-board communications at performance levels scaling to ten Gigabits per second and beyond.

Knowing that verification consumes most of the time in design proces, RapidIO verification component seems to be logical choise if we want to keep the pace with tight schedules and accelerate time-to-market of RapidIO products. HDL Design House RapidIOeVC (HDH 5000) is very adatable and easy to use solution for different user demands in verification of RapidIO devices.

Features

- **RapidIO Interconnect Specification Rev. 1.2 compliant**
- **Fully eRM compliant**
- **Supports Physical 8/16 LP-LVDS Layer Specification, with all packets**
- **Supports Common Transport Layer Specification, with all packet kinds**
- **Supports Input/Output and Message passing Logical Layer Specifications, with all packet kinds**
- **Protocol layers implemented as sub-agents with rich sequence libraries per each**
- **Supports directed, random and erroneous test generation at all protocol layers**
- **Protocol monitoring and checking through common and per sub-agent monitors**
- **Comprehensive built-in coverage model implemented on all protocol layers**
- **HDL independent**

Description

HDH 5000 (RapidIO eVC) implements operation of RapidIO Interconnect Specification compatible devices. It covers full protocol functionality in all three layers: physical, transport and logical. HDH 5000 integrates one RapidIO device (with transmit and receive path), that can drive, receive and respond to all kinds of RapidIO packets driven to RapidIO 8/16 Physical Layer.

A HDH 5000 device consists of three layered sub-agents - each one implementing one protocol layer. Every sub-agent on its transmit path is supported with appropriate sequence and sequence driver. RapidIOeVC (HDH 5000) per layer functionalities are:

- Logical layer agent is responsible for generating sequences and transactions (packets) of Logical Layer RapidIO specification. It includes two implementations of the logical layer: Input/Output Logical Layer Implementation and Message Passing Logical Layer Implementation.

- Transport layer agent is responsible for generating sequences and transactions of Common Transport Layer RapidIO specification.
- Physical layer agent is responsible for generating sequences and transactions of Physical Layer 8/16 LP-LVDS RapidIO specification; it is in charge of setting up connection, packet -retry mechanism, etc...

For each of the data paths, transmit and receive, per layer monitor is available with rich set of protocol checkers and coverage items.

Verification environments

RapidIO eVC (HDH 5000) can be used in module level verification. In such environment, eVC is instantiated and connected to the appropriate DUT interface, as it is shown on figure below. An eVC environment behavior is modeled by defining a library of sequences.

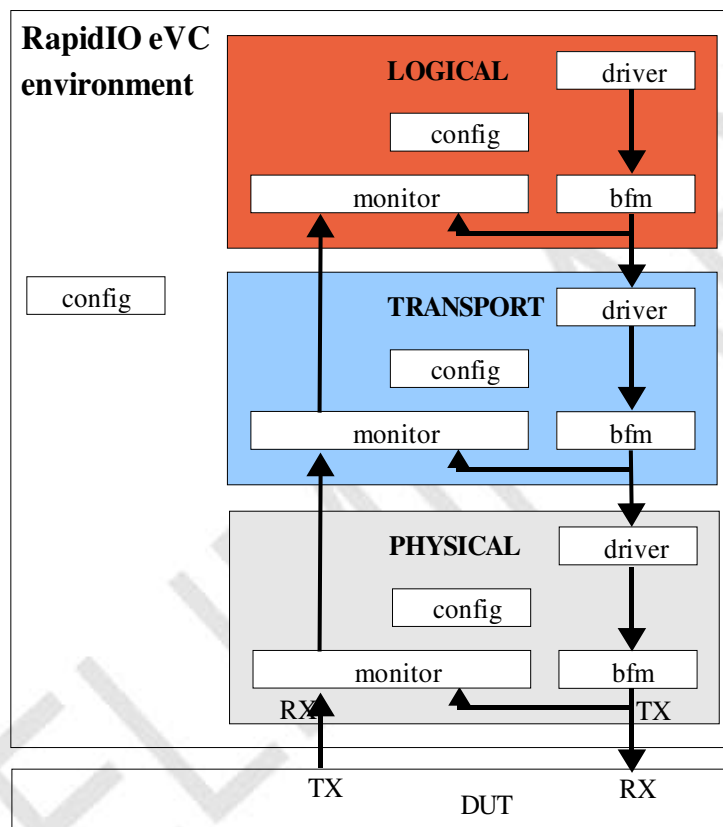


Figure: RapidIO eVC (HDH 5000) in module level verification environment

In addition, HDH 5000 being eRM compliant plug and play component, can be easily integrated into complex SoC verification environment. In both cases, module level or SoC validation process, RapidIO eVC can be configured to run sequences (directed, random, erroneous), report ongoing events on different levels of verbosity, check for protocol violations and support scoreboards.

Applications

- Module level verification for a component with RapidIO interface
- System On Chip level verification

Deliverables

RapidIO eVC (HDH 5000) is delivered in a form of a full eRM package containing:

- HDH 5000 encrypted code
- Complete documentation that includes: User's Guide, Release Notes, Training presentation
- Examples of eVC usage
- Demos for easy feature demonstration

Support

- One month of technical assistance via e-mail is included in the basic price
- The product can be customized according to the customer request
- Full technical support can be arranged
- Different license models

Availability

HDH 5000 (RapidIO eVC), will be available at Q1/05.

Contact Info

HDL Design House is fast growing privately owned company focused on providing re-usable, configurable and synthesizable VHDL/Verilog IP cores for SoC solutions and ASIC and FPGA design and design verification services.

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