

Overview

The process of developing appropriate verification environment for today's system-on-chip (SoC) designs becomes really hard, due to the fact that they include number of different protocols, peripherals, interfaces and processors. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, the reusability in verification has a very significant role. In order to increase verification productivity, huge verification environments are assembled from a number of verification components. Each of the verification components is designed for a specific protocol or architecture and is configured by the environment to produce desired behavior.

Registers package (HDH 4000) represents implementation of register map in e language. HDH 4000 is fully eRM compliant e-language package that can be used in any verification environment that needs to have representation of registers, register maps and register fields. This package supports variable register/field width, access by name/address, and various types of field kinds and reset types. HDH 4000 is standardized, reusable component that can be easily integrated into more complex verification environment.

Features

- Implementation of register map containing registers of different width and different kinds of register's fields
- Fully eRM compliant
- Reading from address inside the register map
- Writing to address inside the register map
- Reading from register, accessing it by its name
- Writing to register, accessing it by its name
- Easy way of register map and registers configuration using macros
- Reading specific register's field accessing it by its name
- Register map reset – COLD and WARM kind of reset supported
- Different kind of fields supported – RO (readable only), RW (readable and writable), RS (readable and settable by writing 1) and RC (readable and clearable by writing 1)

Description

Registers package (HDH 4000) can implement one or more register maps containing different number of registers. These registers can be of different length and fields types.

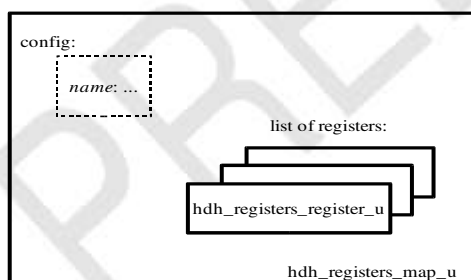


Figure 1: Architecture of the `hdh_registers_map_u`

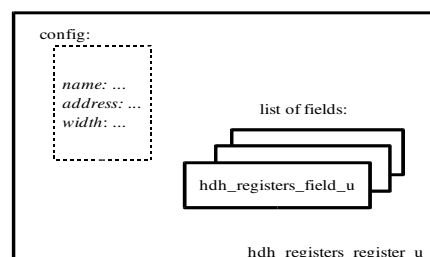


Figure 2: Architecture of the `hdh_registers_register_u`

Verification environments

Registers package (HDH 4000) can be used as a part of an eVC, or as a part of a more complex verification environment.

Applications

- HDH 4000 can be applied on any verification component that should implement register maps.

Deliverables

Registers package is delivered in a form of an eRM package under GNU GPL, containing:

- HDH 4000 open source in e-Language
- Needed documentation: Release Notes, User 's Guide
- Examples of HDH 4000 usage
- Demo for easy features presentation

Support

- This product is distributed under GNU GPL. Support is provided via e-mail: evc_support@hdl-dh.com

Availability

Registers package (HDH 4000) – available right now.

Contact Info

HDL Design House is fast growing privately owned company focused on providing re-usable, configurable and synthesizable VHDL/Verilog IP cores for SoC solutions and ASIC and FPGA design and design verification services.

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