



HDH 3000 I2C - e VERIFICATION COMPONENT (eVC)

HDH 3000 DATASHEET – AUGUST 2004 – VERSION 1.0

Overview

The process of developing appropriate verification environment for today's system-on-chip (SoC) designs becomes really hard, due to the fact that they include number of different protocols, peripherals, interfaces and processors. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, the reusability in verification has a very significant role. In order to increase verification productivity, huge verification environments are assembled from a number of verification components. Each of the verification components is designed for a specific protocol or architecture and is configured by the environment to produce desired behavior.

eVCs are e-Language Verification Components used for verification environments based on Verisity's Specman-Elite tool. They are reusable, configurable, easy to use and integrate into different verification environment. Their development is based on e Reuse Methodology (eRM) defined by Verisity.

I2C eVC (HDH 3000) emulates behavior of I2C bus and it can be used for verification of a single device containing an interface to I2C bus or for a verification of a multiple I2C compatible devices system. HDH 3000 is fully eRM compliant, which makes it easy to use and configure. HDH 3000 is standardized, reusable component that can be easily integrated into more complex verification environment. A single HDH 3000 with appropriate configuration can be used for both single DUT and multiple DUT verification.

Features

- Supports I2C bus specification version 2.1
- Fully eRM compliant
- I2C device types implemented: MASTER, SLAVE, MASTER/SLAVE
- General Call address handling
- Support for 10-bit addressing
- Different speed modes: Standard mode, Fast-mode and High-speed mode (Hs-mode)
- Full control over bus transactions generation using sequences and sequence drivers
- Error and wait states injection
- Scoreboard checking supported
- Built in monitors for protocol checking including a global bus monitor
- Built in coverage analysis for all packet types
- Directed-random test generation
- HDL independent

Description

I2C eVC (HDH 3000) can implement one or more of these functions:

- MASTER: Emulates I2C master device behavior-initiation of all kinds of bus transactions, clock generation, data transmitting/receiving and performs arbitration and clock synchronization.
- SLAVE: Emulates the behavior of I2C slave device behavior-generating responses to all kinds of masters requests, using handshake mechanism for synchronization with faster master.

I2C eVC also performs bus monitoring function that includes detecting and logging of bus transactions, protocol checking and coverage collecting at both single device level and global, bus level.

Verification environments

I2C eVC environment can be used in module level verification. Each DUT with I2C interface can be verified with single I2CeVC, configured appropriately.

I2C eVC (HDH 3000) is fully configurable and easy to use in both module and system level verification. It can be configured to emulate single master, slave or master-slave device but also it can emulate the entire I2C bus system with multiple devices. In both cases, single, appropriately configured component of HDH 3000 is used.

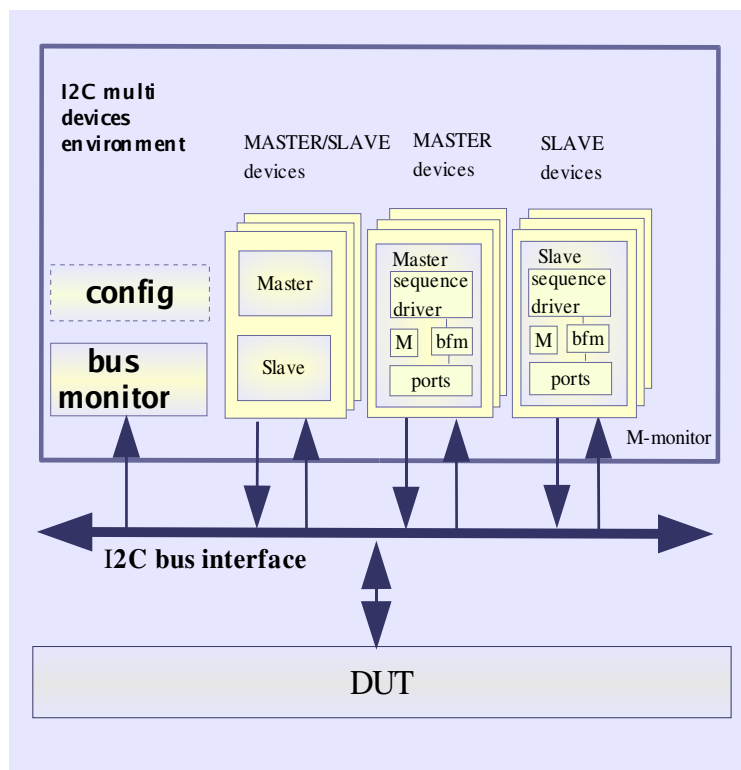


Figure:I2C eVC (HDH 3000) verification environment

I2C eVC (HDH 3000) can be configured in various ways to verify any specific configuration or behavior of DUT. Per instance, for verification of single slave device, HDH 3000 can be configured to emulate behavior of single master device, while for verification of single master device can be used configuration with one master and multiple slave devices:

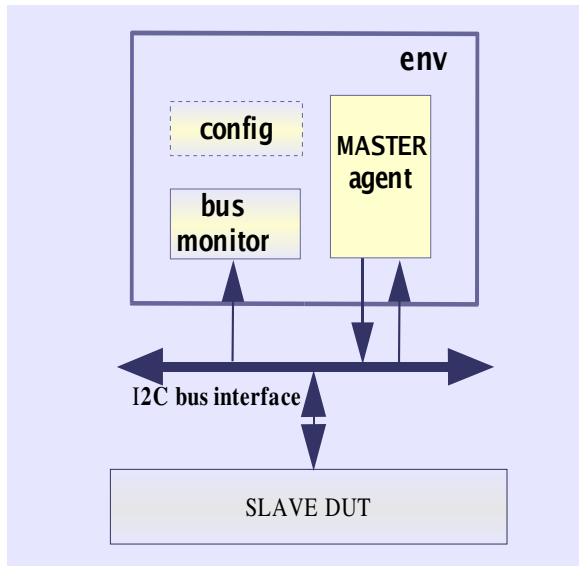


Figure:I2C eVC (HDH 3000) verification environment for verification of single slave device

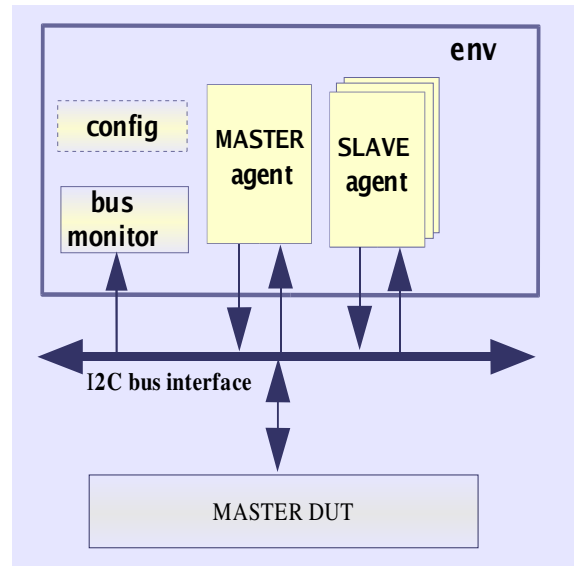


Figure:I2C eVC (HDH 3000) verification environment for verification of single master device

Applications

- Module level verification for a component with a I2C interface
- System On Chip level verification

Deliverables

I2C eVC is delivered in a form of a full eRM package containing:

- HDH 3000 encrypted source in e-Language
- Complete documentation: Release Notes, Training presentation, User 's Guide
- Examples of eVC usage
- Demos for easy feature demonstration

Support

HDL DH offers different levels of customer support.

Basic eVC license:

- 3 months of technical support via email

One year maintenance fees includes:

- all updates of the eVC for the maintenance period
- technical support via email for the maintenance period

Additional support:

- on site support by eVC developers
- eVC redesign according to the customer requirements
- different license models

Availability

I2C eVC (HDH 3000) is available right now.

Contact Info

HDL Design House is fast growing privately owned company focused on providing re-usable, configurable and synthesizable VHDL/Verilog IP cores for SoC solutions and ASIC and FPGA design and design verification services.

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