



HDH 2000

Serial ATA - e VERIFICATION COMPONENT (eVC)

HDH 2000 DATASHEET - JULY 2004 - VERSION 1.0

Overview

The process of developing appropriate verification environment for today's system-on-chip (SoC) designs becomes really hard, due to the fact that they include number of different protocols, peripherals, interfaces and processors. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, the reusability in verification has a very significant role. In order to increase verification productivity, huge verification environments are assembled from a number of verification components. Each of the verification components is designed for a specific protocol or architecture and is configured by the environment to produce desired behavior.

eVCs are e-Language Verification Components used for verification environments based on Verisity's Specman-Elite tool. They are reusable, configurable, easy to use and integrate into a verification environment. Their development is based on e Reuse Methodology (eRM) defined by Verisity.

Serial ATA protocol is a high-speed serial link replacement for parallel ATA interface of mass storage devices. The serial link used is a differential Gigabit technology and 8b/10b encoding. Two parts involved in Serial ATA link are SATA Host and SATA Device. Serial ATA standard defines full protocol stack, from application level down to the physical connection. Being fully compatible with legacy ATA/ATAPI standard, Serial ATA appears as long term mass storage connectivity solution. Serial ATA eVC (HDH 2000) can be used for verification of an IP core containing either host or one or more devices. For SoC verification process, eVC may be easily integrated into more complex environment. HDH 2000 Serial ATA eVC is very adaptable and easy to use solution for different user's demands.

Features

- **Serial ATA rev1.0a / Serial ATA II rev1.1 compliant**
- **Supports legacy ATA commands**
- **Fully eRM compliant**
- **Implements both, host and device (up to 16 devices)**
- **Protocol layers implemented as sub-agents with rich sequence libraries per each**
- **Optional DUT access to physical or link layer**
- **Port Multiplier and Port Selector support**
- **Supports directed, random and erroneous test generation at all protocol layers**
- **Protocol monitoring and checking through common and per sub-agent monitors**
- **Supports scoreboard checking**
- **Comprehensive built-in coverage model implemented on all protocol layers**
- **Port Multiplier Rev1.1 model included**
- **HDL independent**

Description

HDH 2000 (Serial ATA eVC) implements operation of both host and device, for either Serial ATA, or Serial ATA II protocol. It covers protocol functionality up to the application layer and supports legacy ATA commands. A HDH 2000 integrates one global monitor, one host and one or more (Serial ATA II) device agents.

A HDH 2000 agent (host or device) consists of four layered sub-agents everyone implementing one protocol layer. Every sub-agent on its transmit path is supported with appropriate sequence and sequence driver. Two upper layer sub-agents, Application and Transport, are tied to the Transaction and Link sub-agents directly (lower layer sequence pulls data from upper layer sequence driver), while Link and Physical sub-agents contain an appropriate Bus Functional Models for driving signals directly. It is possible, depending on configuration, to drive DUT from Physical or Link layer. Serial ATA eVC (HDH 2000) per layer functionalities are:

- Application layer agent is responsible for generating sequences of legacy ATA commands, handling Shadow Register Block, and in the case of host adapter Status and Control Block of registers.

- Transport layer agent translates requests received from application layer into the Frame Information Structures and transfers them to the Link layer agent. In other direction, the Transport layer agent receives FISs, decomposes them and transfers items to the Application layer agent.
- In transmit path Link layer agent calculates a CRC, adds it to the FIS together with standard frame start and stop primitives. In opposite direction, it checks CRC, and cleans packet from primitives. If configuration allows, this layer may directly drive DUT signals, using its own BFM.
- Physical layer agent is responsible for setting up connection and serialization/deserialization of data.

For each of the data paths, transmit and receive, per layer monitor is available with rich set of protocol checkers and coverage items.

Verification environments

Serial ATA eVC (HDH 2000) can be used in module level verification. In such environment eVC is instantiated as host or device and connected to the appropriate DUT interface, as it is shown on figure below. An eVC environment behavior is modeled by defining a library of sequences.

In order to support partial Serial ATA IP core solutions, HDH 2000 eVC, can be configured to run from Application layer down to Link layer, where it is connected to DUT. In such configuration DUT, on its serial link boundary, is connected to the other Serial ATA eVC (HDH 2000) agent. In opposite case, if DUT implements upper three SATA layers verification environment should be configured to connect Physical layer HDH 2000 sub-agent on one side to the eVC agent, and on the other to the DUT driving Link layer signals.

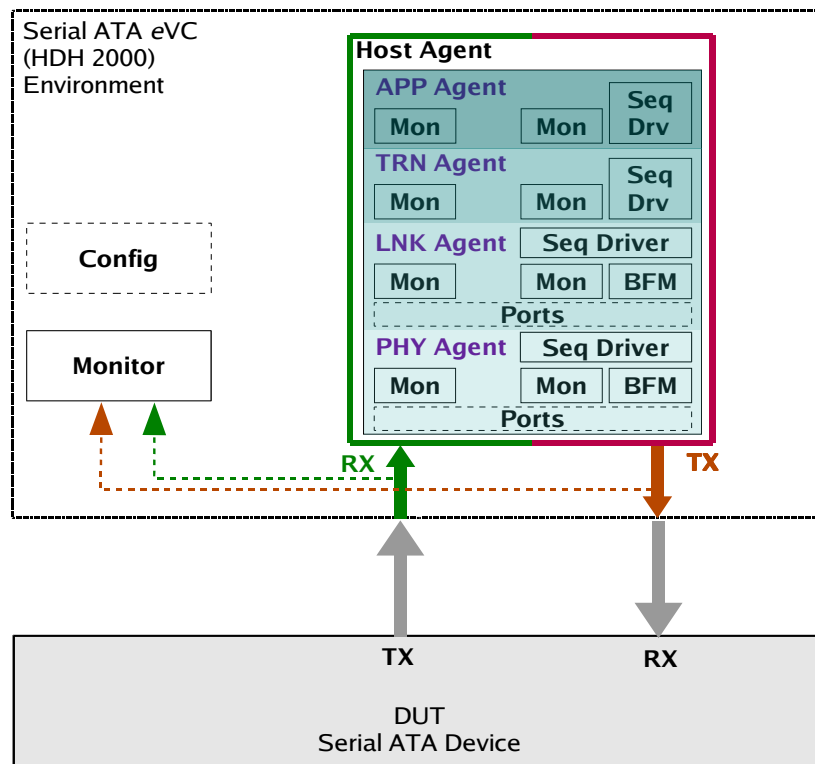


Figure: Serial ATA eVC (HDH 2000) in module level verification environment

In addition, HDH 2000 being eRM compliant plug and play component, can be easily integrated into complex SoC verification environment. In both cases, module level or SoC validation process, Serial ATA eVC can be configured to run sequences (directed, random, erroneous), report ongoing events on different level of verbosity, check for protocol violations and support scoreboards. It also includes Port Multiplier Specman model that can be easily integrated into existing verification environment.

Applications

- Module level verification for a component with Serial ATA interface.
- System On Chip level verification.

Deliverables

Serial ATA eVC (HDH 2000) is delivered in a form of a full eRM package containing:

- HDH 2000 encrypted code
- Complete documentation that includes: User's Guide, Release Notes, Training presentation
- Examples of eVC usage
- Demos for easy feature demonstration

Support

HDL Design House offers different levels of customer support.

- Basic eVC license:
 - 3 months of technical support via e-mail
- One year maintenance fees includes:
 - All updates of the eVC for the maintenance period
 - Technical support via e-mail for the maintenance period
- Additional support:
 - On site support by eVC developers
 - eVC redesign according to the customer requirements
 - Different license models

Availability

HDH 2000 (Serial ATA eVC), will be available by end of Q2/04.

Contact Info

HDL Design House is fast growing privately owned company focused on providing re-usable, configurable and synthesizable VHDL/Verilog IP cores for SoC solutions and ASIC and FPGA design and design verification services.

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