



e Verification Component Suite

UART eVC

▶ e Verification Components

Globetech Solutions' eVCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Verisity's Specman Elite™ testbench automation tool, these components can provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

▶ e Reuse Methodology

Globetech Solutions' eVCs comply with Verisity's e Reuse Methodology (eRM™). The eRM ensures that eVCs seamlessly plug-and-play and operate consistently with all eRM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.



▶ Why eVCs?

There are many advantages to choosing a Globetech Solutions e Verification Component:

Time to silicon - dramatically reduce the verification cycle

Flexibility - quickly create and fine tune a variety of test scenarios

Risk Management - pre-verified components help reduce problem space

Re-usability - spend your time creating new tests, not environments!

Full Support - integration, training and support to ensure your success

▶ The UART eVC

The UART (Universal Asynchronous Receiver Transmitter) eVC is a powerful verification bundle built around the UART industry standard. Adopted by companies worldwide as a building block for reusable verification platforms, the UART eVC can be integrated in a variety of testing scenarios involving a processor and modem/network, making it ideal for embedded processor applications or System-on-Chip (SoC) environments.

▶ Features

- Compatible with industry standard UART devices
- Written in e and fully compatible with Specman Elite - HDL independent
- eRM and VPA compatible - Plug-n-Play
- Serial interface agent provides constrained-random UART frame sequence generation with error injection
- Programmable serial interface characteristics with auto-flow support
- Independent monitor supports re-usability in different verification environments without loss of coverage
- Extended data and protocol checkers for UART 16x50 devices with arbitrary FIFO sizes
- Processor *Driver Abstraction Layer* architecture provides high-level generation tools for test writing and monitoring, irrespective of processor interface and device implementation
- Independently controlled and fully prioritized interrupt handling and DMA support
- Built-in coverage analysis for Coverage-Driven Verification (CDV)
- Complete and configurable error reporting, adjustable levels of tracing and verbosity

▶ UART eVC Structure

The UART eVC can comprise two to four main modules: the UART Agent, the Monitor, the 16550 core, and the Processor Driver. This structure allows for maximum flexibility in designing testing scenarios, as well as scalability, control and isolation (Table 1).

▶ Verification using the UART eVC

The UART eVC comes in two different implementations whose extended capabilities make it easy to exercise a variety of designs-under-test, providing full metrics for error conditions and functional coverage.

In **Figure 1**, the generic UART eVC is used to verify the UART interface of a larger device under test. In this scenario, the serial UART agent initiates constrained-random sequences to the DUT. The *monitor* examines traffic, scoreboards data and utilizes the *checker* for adherence to the UART protocol. The *coverage* module ensures that all aspects of the protocol are exercised. The eVC makes no assumptions as to the internal device's architecture or processor interface, making it applicable to virtually any type of UART device.

In **Figure 2**, the UART 16x50 eVC is used in a **core-level** verification scenario of a 16x50 (fast) UART device. Both the serial and the processor drivers initiate transactions to the DUT by means of the dual drivers available. The *monitor* examines traffic not only on the serial but also on the processor interface, providing for interface cross-checking, device-level verification and functional coverage collection capabilities. Finally, the 16x50 core includes a full UART 16550A implementation that can be used for familiarization or early access to system-level verification activities.

In conclusion, employing the UART eVC in your current design verification, ensures that you will have available a solid tool based on an industry standard protocol that can be re-used for future projects.

▶ Licensing

Globetech Solutions eVCs are distributed with a simple floating license, which allows for multiple eVC instantiations. Each Specman Elite license requires a separate eVC license.

▶ Further Information



For further information, visit www.globetechsolutions.com. In addition, you can email us at info@globetechsolutions.com or call ++1 650 988 6900 (US) or ++30 23 10 31 35 53 (Europe)

Component	Function
UART Agent	Emulates the corresponding functionality of the serial device attached to the UART DUT by injecting data and control stimuli.
Monitor	Tracks activity on the network side of the UART device. It also provides error checking, data scoreboarding and coverage information. In the 16x50 edition, the monitor also provides interface cross-checking across the UART device.
Core <i>16x50 version only</i>	A complete UART 16X50 core in e. It can be used in place of DUT for training and familiarization, as well as advanced verification scenarios. The core can also be used in place of a UART DUT.
Processor Driver <i>16x50 version only</i>	This component emulates the processor behavior at the device level. It provides stimuli to the DUT, in the form of register reads and writes, creating a continuous data and control exchange path.

Note that the monitor element is required for all testing scenarios; all other elements are entirely independent and can be deployed separately.

Table 1: Functional Description of UART eVC Components

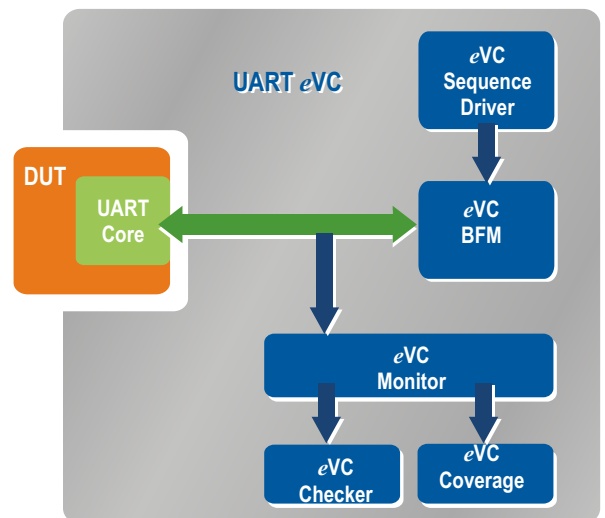


Figure 1: Verification Using the UART Interface-Level eVC

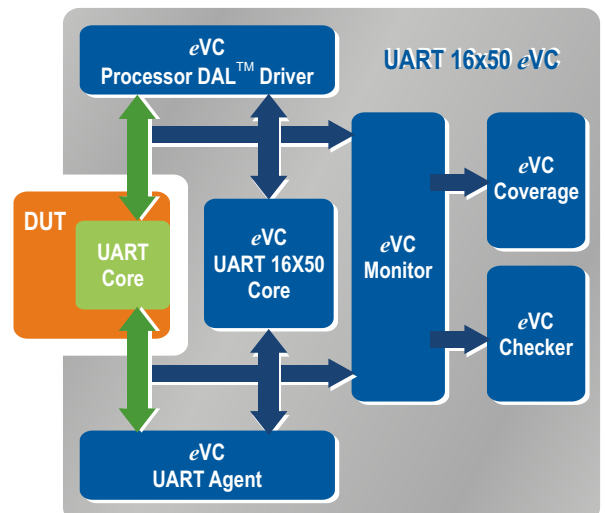


Figure 2: Verification Using the UART 16x50 Core-Level eVC