Black Cat Electronics Ethernet eVC

Ethernet *e*VC

Overview

eVC's are reusable and highly configurable verification components targeted at users of Verisity's Specman Elite™ functional verification tool.

The Ethernet ***e***VC from Black Cat Electronics is an off-the-shelf verification component for the functional verification of core and SoC designs incorporating Ethernet MAC and PHY layer interfaces. All speeds of physical medium are supported from 10Mbps to 10Gbps.

The Ethernet ***e***VC provides a simple yet extremely powerful user interface that allows verification engineers to rapidly develop verification environments for designs containing Ethernet functionality. The Ethernet ***e***VC can be used both for IP development and for IP integration. IP suppliers can also use the Ethernet ***e***VC to deliver integration toolkits to IP integrators.

Features·

- Compliant to ISO/IEC 8802-3:2000(E) Specification.
- Uses 'virtual medium' technology to model single and multiple Ethernet stations on a medium, allowing easily generation of realistic traffic patterns.
- Supports both point-to-point and shared media.
- Supports multiple DUT (Device Under Test) instances on the same virtual medium enabling end-to-end system level testing.
- Simple yet extremely powerful test interface allows control over all aspects of ***e***VC behaviour and promotes re-use of test code.
- Individual control of configuration and traffic patterns for each device model.
- Duplex mode and network speed can be reconfigured during test.
- Full support for auto-negotiation.
- Mandatory station management registers are modelled for each interface type. Fully programmable station management register model is available for non-mandatory registers.
- Station management registers can be accessed both via MDIO interface and through test interface.
- Fully controllable interface-level symbol error insertion allows testing of error detection/correction mechanisms under realistic scenarios.
- Comprehensive support for MAC frame formats including data frames, pause frames and VLAN frames.
- Comprehensive mechanism for generation of illegal/errored frames.
- Protocol error generation mechanism.
- Configurable log file production (for data-path and station management) with test statistics.

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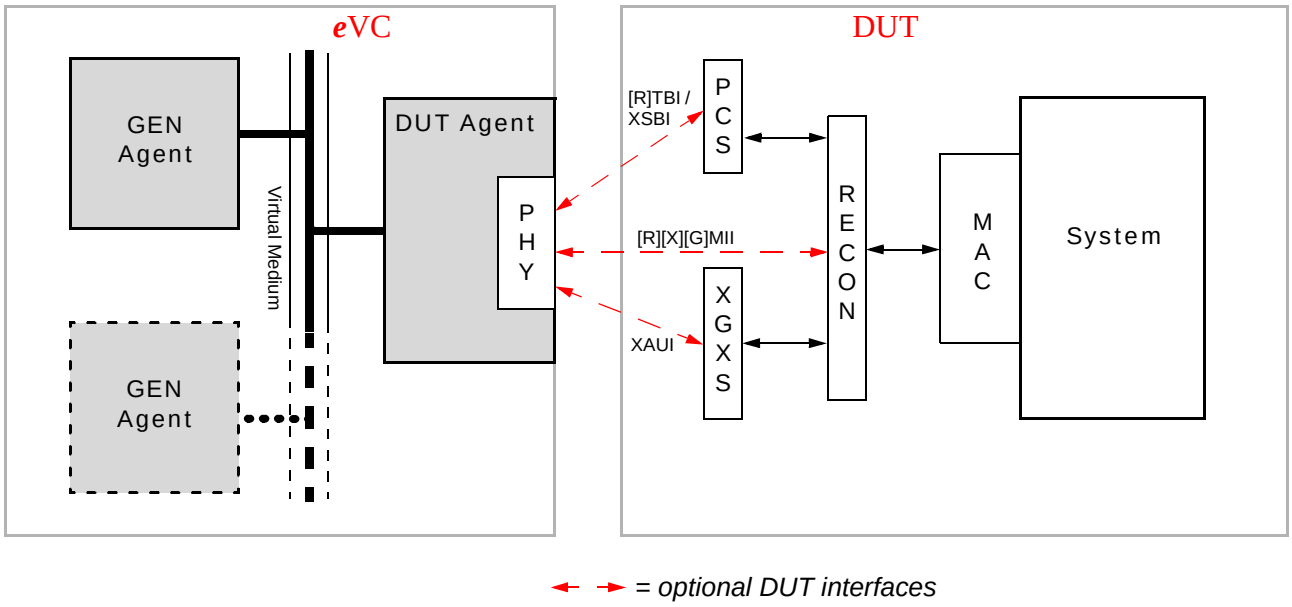
Figure 1. *e*VC Structure and Verification Environment



- Comprehensive mechanism for trace/debug of ***e***VC behaviour.
- Extensible coverage collection.
- Full protocol checking of data-path and station management interface.
- Scoreboarding hooks provided along with simple generic homogeneous scoreboard.
- Utilises latest ***e***VC methodology to ensure full compatibility and inter-operability with other ***e***VCs.
- Comprehensive documentation and support.

eVC Structure

Figure 1 illustrates the components of the Ethernet ***e***VC and the possible DUT interfaces.

The ***e***VC internal structure is highly user configurable. Within the ***e***VC there is a single instance of a *Virtual Medium*. There can be multiple instances of both *GEN Agents* and *DUT Agents* controlled by the user.

GEN Agent(s)

GEN Agents are traffic generators that inject MAC data frames or variants (such as VLAN or pause frames) onto the Virtual Medium. Frames are sent over the Virtual Medium as abstract data structures allowing virtual control data to be attached.

The GEN agents can be dynamically disconnected and re-connected during test.

When operating in Full Duplex mode, the GEN Agents can both originate and respond to Pause frames.

When operating in Half Duplex mode, the GEN Agents handle deferral, and collision back-off.

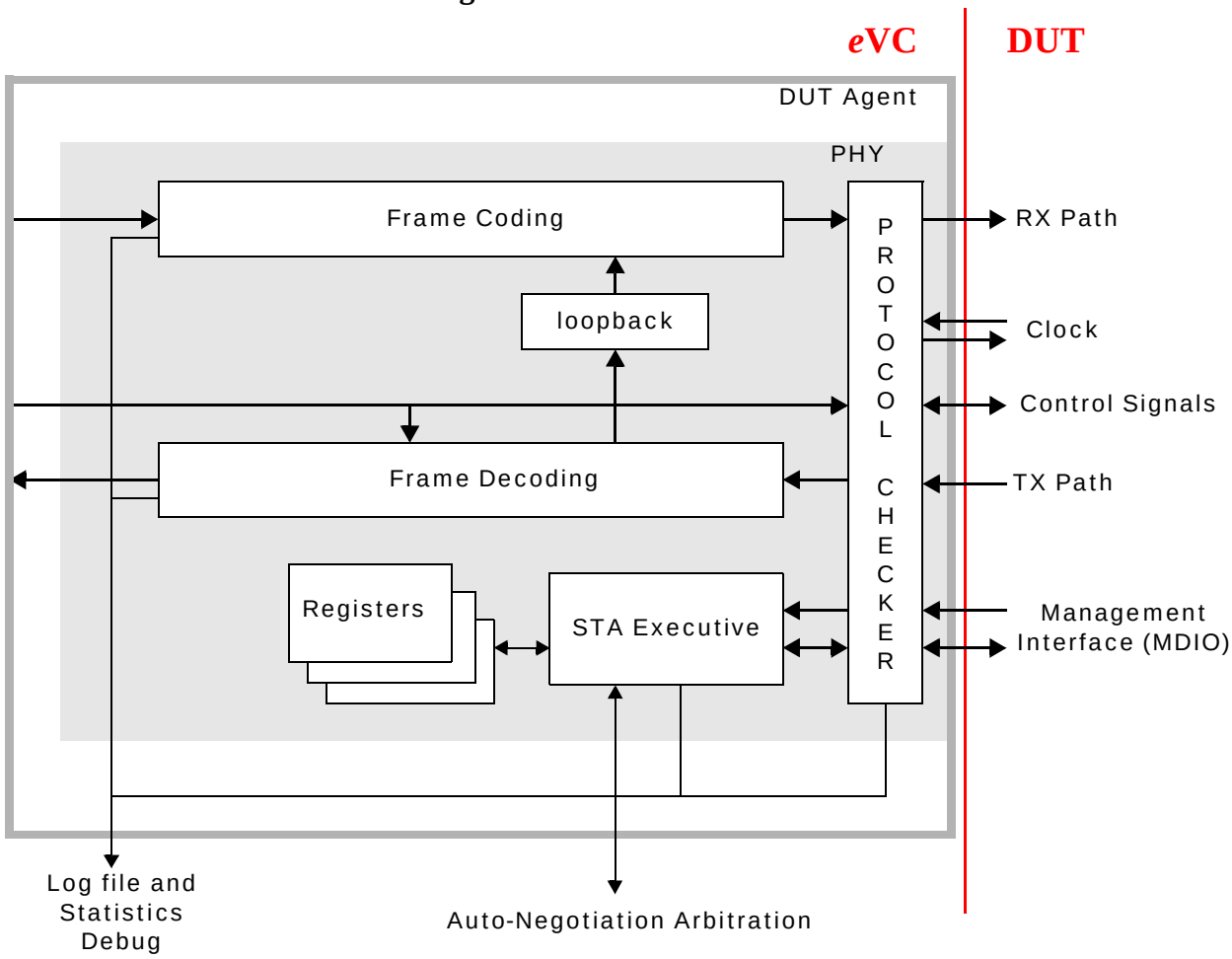
The GEN Agents use a highly extensible sequence-based generation scheme that allows co-ordination of test generation between multiple GEN Agents, multiple Ethernet ***e***VC instances and even multiple different ***e***VCs.

The frame structure provides virtual control fields that allow a comprehensive variety of errors to be introduced.

Virtual Medium

The Virtual Medium provides a high-level model of the Ethernet CSMA/CD algorithm and provides the mechanism by which one or more GEN Agents are connected to one or more DUT Agents. There is only one instance of the Virtual Medium per instance of the ***e***VC but the ***e***VC can

Figure 2. PHY Structure



be instantiated multiple times in a verification environment for a single license. The Virtual Medium allows modelling of traffic patterns in a single collision domain.

When operating in Full Duplex mode, the Virtual Medium simply acts as a bidirectional transport between two Agents connected to it.

When operating in Half Duplex mode, the Virtual Medium is capable of fully modelling collision domain behaviour. The collision domain is modelled as a linear 'virtual medium' and the connection point of each Agent is specified in terms of the propagation delay relative to an arbitrary 'origin'. GEN Agents only generate each frame at the time where it is required by the DUT Agent - this allows frame generation to react to the current states of both the verification environment and the DUT. However, collision modelling is performed based on the specified medium propagation delays allowing a full range of collision behaviours to be modelled.

DUT Agent(s)

The DUT Agent provides the interface between the Virtual Medium and a PHY layer (or part PHY layer) model that provides connectivity to the DUT.

Normally there is a single DUT Agent per instance of the ***e***VC. However, two or more DUT Agents may be used to provide 'back-to-back' testing of DUTs.

In Half Duplex mode, the DUT Agent is capable of handling collision fragments created by the Virtual Medium and passing these accurately to the DUT.

PHY Models

A range of PHY layer models are provided to allow connection of the ***e***VC to the DUT via a variety of different signal interfaces. Each DUT Agent is configured for a specific PHY layer model for a given test.

Figure 2 shows the structure of the PHY model.The PHY model provides translation between high level frame descriptions (as generated by the GEN Agents and propagated by the Virtual Medium) and the low level interface at the DUT.

The Frame Decoder reconstructs high-level frames from the DUT interface and classifies them according to the level and type of errors encountered.

The Protocol Checker monitors the data-path and station management signals to and from the DUT at both low and high levels.

The various components of the PHY layer collect coverage and logging information and generate statistics.

Station Management

The PHY element also models the station management interface and the associated register sets. There is a Station Management Executive within the PHY to control the DUT access to the register sets via an 'MDIO' interface. It is also possible for the verification environment to directly read and write the contents of the STA registers.

All mandatory registers for each kind of PHY are implemented to both reflect and affect the internal state of the ***e***VC PHY model. Optional registers can be modelled or restricted under user control.

For point-to-point networks, auto-negotiation is fully modelled with provision made for specifying the parameters of both the local PHY and the link-partner PHY. These parameters can be changed dynamically during the test.

Full coverage and logging of the Station Management interface and registers is provided.

Scoreboarding

Flexible scoreboard hooks are provided in the DUT Agent to allow implementation of end-to-end scoreboarding in the user verification environment. For designs where data flow is from Ethernet frame to Ethernet frame (e.g. routers, switches, hubs, etc.), a generic homogeneous scoreboard model is provided.

Supported PHY Interfaces

- MII (10Mbps and 100Mbps)
- GMII
- RMII (10Mbps and 100Mbps)
- RGMII
- TBI
- RTBI
- XGMII
- XAUI
- XSBI

Others can be supplied by arrangement.

Company Background

Black Cat Electronics is a world leader in ***e***VC methodologies and is currently working closely with Verisity on the development of a new generation of ***e***VC methodology.

The Ethernet ***e***VC is the first of a family of ***e***VC products due to be launched by Black Cat Electronics in 2002.

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