

Ethernet *e*VC

Automated, Coverage-Driven Verification IP

Ethernet *e*VC

- ✓ Supports MII, GMII, RMII*, SGMII*, SMII*, TBI, XGMII, XAUI, XSBI interfaces (for applicable bandwidths)
- ✓ Compliant to ISO/IEC 8802-3:2000(E) and P802.3ae/D4.0 Specifications
- ✓ Simulates single or multiple Ethernet devices on a medium, generating and collecting Ethernet packets
- ✓ Supports 10 Mb, 100 Mb, 1 Gb, 10 Gb bandwidths
- ✓ Supports Ports capable of Full Duplex or Half duplex mode
- ✓ Supports the management interface for all supported interfaces
- ✓ Supports configuration of different ports independently (Switch configuration for example, 10 and 100 Mbps port in one switch)
- ✓ Monitors protocol and reports violations
- ✓ Users can control generation of transactions for each device model
- ✓ Fully supports *e*RM features such as message(), sequences, packaging and naming conventions
- ✓ Extensive sequence library for developing advanced sequences
- ✓ Fully configurable error generation allows testing of error detection mechanisms under realistic scenarios
- ✓ Utilizes *e*RM methodology to ensure compatibility and inter-operability with other *e*VCs

* RMII consortium 1998 (Revision - 1.2)

* SMII - Cisco systems (Revision - 2.1)

* SGMII - Cisco systems (Revision - 1.7)

e Verification Component Overview (*e*VC)

e Verification Components are reusable, configurable, pre-verified, plug-and-play verification environments. They offer the easiest to use, most complete module, chip and system level verification solution available. *e*VCs integrate automatic stimulus generation, assertion checking, and functional coverage analysis all within a single, extensible component. *e*VCs drastically reduce the time needed to compose a verification environment.

The philosophy underlying *e*VCs differs significantly from alternative products. Rather than use thousands of directed tests, the *e*VC employs automatic generation and a coverage driven methodology. Using automated scenario generation the *e*VC can typically achieve 90-95%+ coverage of the protocol. With the addition of a few tests the remaining corner cases are then exercised. This approach uncovers more bugs faster and frees engineering time to focus on testing the Device Under Test (DUT) proprietary functionality.

Quality and Productivity Gains

With *e*VCs verification environments are created in days instead of weeks or months. You can begin running tests much earlier and achieve a much higher quality product. Furthermore, *e* Verification Components can be reused without expending any

extra effort. This enables you to retain your investment when moving from module to system level verification as well as when verifying derivative products.

Ethernet *e*VC Overview

The Ethernet *e*VC can be used to verify any IEEE802.3:2000 and IEEE Draft P802.3ae/ D4.0 compliant MAC or PHY device. The *e*VC can be used for the functional verification of IP cores and SoC designs incorporating Ethernet MAC and PHY layer functionality and can be configured to have an unlimited number of Ethernet ports, each interfacing with one of the DUT's Ethernet ports. It works with all HDL simulators that are supported by Specman Elite.

Configurable Verification Environment

The *e*VC can be configured for various types of environments and many different interfaces. Examples include:

- Multi-port MAC Switch environment having either homogeneous or heterogeneous port
- Single/Multi Port MAC Device having any interface
- Single/Multi Port PHY Device

The *e*VC supports the MII, GMII, RMII, SGMII, TBI, XGMII, XAUI, and XSBI interface.

Deliverables

- Fully verified *e*RM compliant Ethernet *e*VC code in encrypted form
- Documentation - User guide and release notes
- Test Suite with comprehensive sequence library

Ethernet eVC

Verity – Meet your SpeX

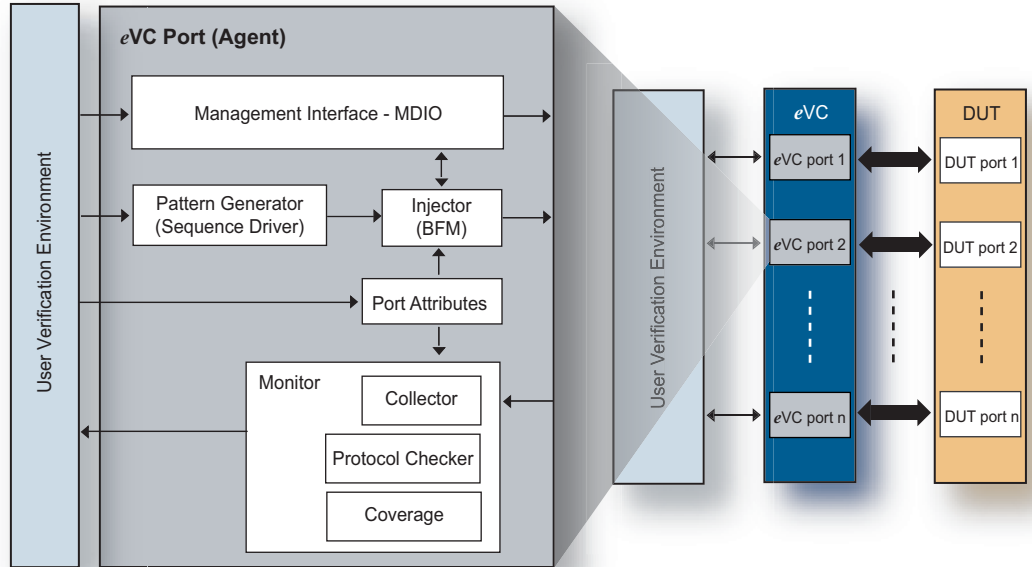
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For More Information

To find out more about the Ethernet eVC contact your Verity account manager or see us on the web at www.verity.com.



Overview of the Ethernet e Verification Component

Ethernet eVC Functional Description

Monitor	Collects the data and detects errors. Monitors the DUT signals, checks for correct protocol behavior and collects coverage.
Pattern Generator	Constrained random sequence based data generation with conditional on the fly data generation (an eRM compliant sequence driver)
Injector	Injects normal and/or erroneous data generated by the pattern generator (an eRM compliant BFM)
Port Attributes	Configures the eVC port operation.
Management Interface - MDIO	Management of Control and Status Registers.

Protocol Checkers, Coverage and the Management interface (MDIO) can be used selectively without any affect on the rest of the eVC's functionality.

