

# AXI *e*VC

## Automated, Coverage-Driven Verification IP

### AXI *e*VC

- ✓ AMBA AXI Bus Specification Revision 1.0
- ✓ Functions as:
  - Master(s)
  - Slave(s)
  - Interconnect monitor
- ✓ Supports any valid AXI topology
- ✓ Supports multiple bus widths
- ✓ Supports the Low Power Interface
- ✓ Supports all valid burst types
- ✓ Supports loop-back mode
- ✓ Total control over bus traffic generation
- ✓ Total control over channel timing
- ✓ Directed and random test generation
- ✓ Built-in bus traffic monitor
- ✓ Built in Interconnect monitor
- ✓ Built-in coverage analysis
- ✓ Scoreboard data checking hooks at all interfaces
- ✓ HDL independent

### *e* Verification Component Overview (*e*VC)

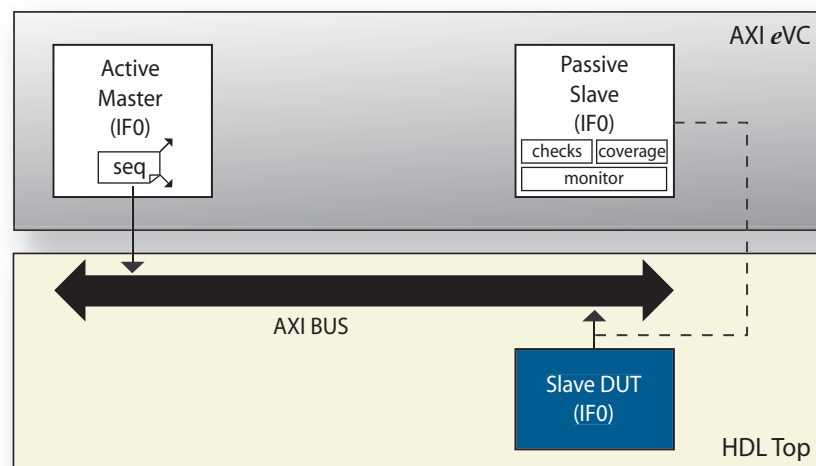
*e* Verification Components are reusable, configurable, pre-verified, plug-and-play verification environments. They offer the easiest to use, most complete module, chip and system level verification solution available. *e*VCs integrate automatic stimulus generation, assertion checking, and functional coverage analysis all within in a single, extensible component. *e*VCs drastically reduce the time needed to compose a verification environment. The philosophy underlying *e*VCs differs significantly from alternative products. Rather than use thousands of directed tests, the *e*VC employs automatic generation and a coverage driven methodology. Using automated scenario generation the *e*VC can typically achieve 90%+ coverage of the protocol. With the addition of a few tests the remaining corner cases are then exercised. This approach uncovers more bugs faster and frees engineering time to focus on testing the DUT's proprietary functionality.

### Quality and Productivity Gains

With *e*VCs verification environments are created in days instead of weeks or months. You can begin writing tests much earlier and achieve a much higher quality product. Furthermore, *e* Verification Components can be reused without expending any extra effort. This enables you to retain your investment when moving from module to system level verification as well as when verifying derivative products.

### AXI *e*VC Overview

The AXI *e*VC is the only automated, coverage driven verification IP available. It comes from Verisity, the leading experts on functional verification. The AXI *e*VC verifies a device under test (DUT) in the AMBA AXI bus environment. It supports the verification of all types of bus based devices including masters, slaves and interconnect, and provides data generation, protocol checking and functional coverage. Verisity and ARM have worked closely together to ensure that the AXI *e*VC accurately verifies the AMBA AXI protocol.



Block Diagram of the AXI *e* Verification Component  
(Single AXI slave DUT with no interconnect)

# AXI eVC

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## Contact Information

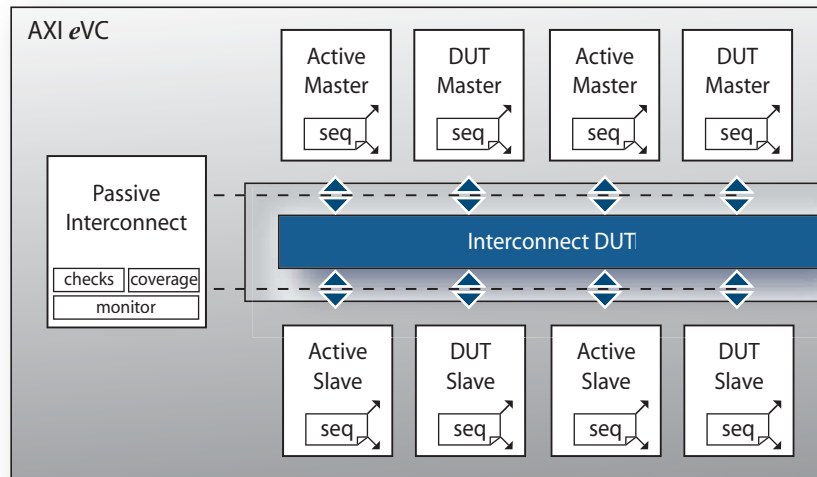
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## For More Information

To find out more about the AXI eVC contact your Verity account manager or distributor.



Block Diagram of the AXI e Verification Component  
(System-Level-AXI DUT environment)

### Overview (continued)

Unlike HDL and C based BFM solutions, the AXI eVC encapsulates Verity's Coverage Driven Verification methodology (CDV). The eVC includes a powerful automatic random sequence generator that automatically creates 90%+ of AXI transactions and responses. The eVC's built-in functional coverage model provides clear reporting of what has and has not been covered. This frees engineers to focus on verifying coverage holes and the DUT's proprietary functionality, integration issues, corner cases and error scenarios.

### Highly Configurable Verification Environment

The eVC can be used for functional verification of AXI devices such as end points and root complexes. Generation of every transaction type for all three AXI layers is fully supported. The eVC can also be configured to selectively enable or disable each layer, each functional block, as well as the functional coverage and checking mechanisms.

## AXI eVC Functional Description

Master	Active emulation of a master device that generates and drives transactions into the bus
Slave	Active emulation of a slave device accepts transaction from any master
Interconnect monitor	Passive monitoring, checking and collection of functional coverage specifically targeted at the AXI interconnect
Monitor	Passive monitoring, checking and collection of functional coverage of bus traffic

