

# SPI 4.2 eVC

## Overview

The SPI-4.2 eVC is a fully documented, off-the-shelf component for users of Verity's Specman Elite™ functional verification environment.

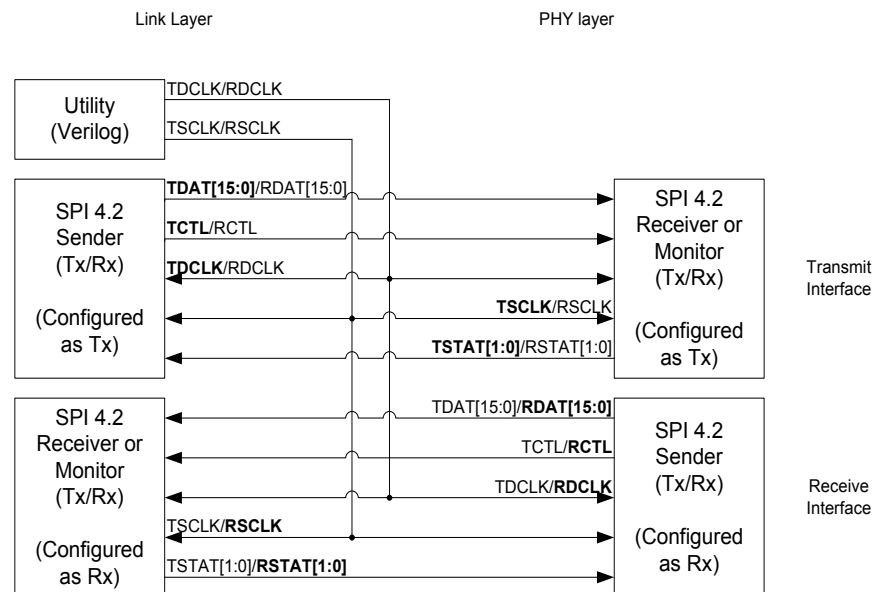
SPI-4.2 is a physical-layer protocol supporting transmission of any kind of payload on up to 256 ports at rates up to 10 Gbit/s. The Cold Spring SPI-4.2 eVC additionally includes implementations of Ethernet, PPP, and ATM.

eVCs are configurable, reusable verification components written in the e language and designed to simplify and speed the verification task. Since with increasingly complex designs verification can take up to 70% of development time, and schedule slips of as little as two months can cost up to 40% of potential lifetime revenues, eVCs provide a tremendous cost and time-to-market advantage.

## Features

- Fully compliant to Optical Internetworking Forum (OIF) Serial Packet Interface Level 4, Phase 2, January 2001
- Simple but powerful and well-documented interface supports both very rapid application and long-term reuse of tests
- Configurable number of ports
- Configurable port arbitration
- Configurable maximum burst size (MAXBURST1, MAXBURST2) per port
- Configurable DATA\_MAX\_T for both sender and monitor
- Configurable FIFO\_MAX\_T for both receiver and monitor
- Configurable CALENDAR, CALENDAR\_LEN, CALENDAR\_M

*The SPI-4.2 mediates between the link and the MAC sublayer of the PHY. In the configuration shown below, the Device Under Test (DUT) could either be either the right or the left side of the drawing. Please note that the monitors shown below include full protocol checking capability.*



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## **SPI-4.2 Features, continued**

- Configurable ALPHA
- Configurable gap between bursts
- Configurable status generation, either automatic or manual mode
- Configurable number of iterations of the status training pattern (high bandwidth)
- Configurable status bandwidth
- Configurable training patterns for data path and status path (high bandwidth) to allow corruption of training
- Configurable synch and loss of synch for both sender and receiver (using DIP-2 for the sender and DIP-4 for the receiver)
- Configurable to insert reserved control words
- Generation of Ethernet II or Ethernet 802.3, ATM UNI or ATM NNI, PPP, or random packets, with automatic or user-controlled content for all frame/packet fields.
- Error injection: Payload control not followed by data; suppress SOP; too-frequent SOPs; suppress EOP, DIP-4 error
- Error injection for data: All fields accessible by user; bad length/type, CRC error mask, optionally remove CRC, set number of CRC errors per million.

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*Cold Spring Engineering is a verification products and services company focused on FPGA, ASIC, and SoC design verification. Our products, IP, and services range from test planning through verification execution to test report generation, all based on tested, reusable verification components. We work with tools from Verisity, Cadence, Synopsys, and Model Technology. Our IP is in C++, and we are equally at home in Verilog and VHDL. For more information, please contact Ben Tsuruda ([btsuruda@coldspringeng.com](mailto:btsuruda@coldspringeng.com)) or Jim Kornell ([jkornell@coldspringeng.com](mailto:jkornell@coldspringeng.com)).*